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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO..
09/749,725	12/28/2000	James S. Burns	2207/10120	6772

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EXAMINER	
LI, AIMEE J	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 12/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/749,725	BURNS ET AL.	
	Examiner	Art Unit	
	Aimee J Li	2183	

-- The MAILING DATE of this communication appears on the cov r sh t with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 October 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4-8,10-15,17 and 18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-8,10-15,17 and 18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1, 2, 4-8, 10-15, 17, and 18 have been examined. Claims 1, 7, and 13 have been amended as per Applicant's request.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: RCE as received on 12 October 2004 and Extension of time for 3 months as received on 12 October 2004.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1, 2, 4-8, 10-15, 17, and 18 are rejected under 35 U.S.C. 102(b) as being anticipated by Hirata et al., U.S. Patent Number 5,430,851.

5. In regard to claim 1, Hirata et al. disclose a processor (col. 4, line 50), comprising:

   a. A plurality of pipelined functional units for executing instructions (Fig. 3, elements 16-18);

   b. A scheduler (Fig. 4, instruction setup units 34 and instruction schedule unit 35 [col. 9, lines 36-45]), coupled to the plurality of functional units (fig. 4, 16-18), programmed for independently mapping instructions, received from at least two separate instruction groups, to at least a portion of the functional units (independent instruction setup units for each instruction stream [col. 5, lines 55-

59] map instructions to functional units by setting a type tag T [col. 6, lines 19-20, 25-27]) during a first stage (fig. 4, instruction setup units 34 comprise of the first stage).

c. Centralized dispersal logic within the scheduler to deliver the instructions to the at least a portion of the functional units via an operation bus (column 4, lines 52-54; column 5, lines 440-43; column 6, lines 11-14 and 25-34; Figure 2(a); Figure 2(b); and Figure 3)

d. Wherein the scheduler is programmed to merge (col. 6, lines 11-14, instruction schedule unit merges the instructions from each of the instruction groups) and remap (col. 8, lines 48-56, instruction schedule unit remaps the instructions based on resource conflicts) a plurality of instruction subgroups, each subgroup from a respective separate instruction group (col. 9, lines 46-64: the instruction schedule unit 35 receives an instruction subgroup of up to 2 instructions from the instruction stream being fetched), to at least a portion of the functional units, based on functional unit requirements and availability (signal R, col. 6, lines 54-56), during a second stage (fig. 4, instruction schedule unit 35 comprises of a second stage).

6. In regard to claim 2, Hirata et al. further disclose that the scheduler is programmed to deliver the instruction to the portion of functional units following merging and remapping (instructions are sent to the functional units from the instruction schedule unit 35 which is responsible for the merging and remapping, fig. 4 and col. 8, 51-56).

7. In regard to claim 4, Hirata et al. further disclose that the functional units execute an increased number of instructions operating at a given clock rate (col. 2, lines 61-64).

8. In regard to claim 5, Hirata et al. further disclose that the instruction groups (instruction streams) follow a simultaneous multi-threading structure (col. 2, lines 65-68).

9. In regard to claim 6, Hirata et al. further disclose that the instruction groups are prioritized to prevent pipeline failures (resulting from contention) during execution of instructions (col. 7, 65-68; col. 8, 1-10).

10. In regard to claims 7 and 13, Hirata et al. disclose a method of dispersing instructions (instruction schedule unit distributes instructions to the functional units, col. 6, lines11-14) to be executed by a processor (col. 4, line 50), comprising:

a. Mapping instructions (instruction setup units [fig. 4, 34] map instructions to functional units by setting a type tag T [col. 6, lines 19-20, 25-27]), received from at least two separate, independent instruction groups (instruction streams, col. 5, lines 55-59), to at least a portion of a plurality of pipelined functional units during a first stage (instruction setup unit 34);

b. Merging (col. 6, lines 11-14, instruction schedule unit merges the instructions from each of the instruction groups) and remapping (col. 8, lines 48-56, instruction schedule unit remaps the instructions based on resource conflicts) a plurality of instruction subgroups, each subgroup from a respective separate instruction group (col. 9, lines 46-64: the instruction schedule unit 35 receives an instruction subgroup of up to 2 instructions from the instruction stream being fetched), to at least a portion of functional units, based on functional unit

requirements and availability (signal R, col. 6, lines 54-56), during a second stage (instruction schedule unit 15);

c. Wherein the instructions are delivered to the instructions to the plurality of functional units using centralized dispersal logic within a scheduler of the processor, via an operation bus (column 4, lines 52-54; column 5, lines 440-43; column 6, lines 11-14 and 25-34; Figure 2(a); Figure 2(b); and Figure 3).

11. In regard to claims 8 and 14, Hirata et al. further disclose the step of delivering the instructions to portions of functional units following merging and remapping (instructions are sent to the functional units from the instruction schedule unit which is responsible for the merging and remapping, fig. 4 and col. 8, 51-56).

12. In regard to claims 10 and 15, Hirata et al. further disclose that the step of merging and remapping includes merging and remapping the instructions to the portion of functional units to allow execution of an increased number of instructions at a given clock rate (col. 2, lines 61-64).

13. In regard to claims 11 and 17, Hirata et al. further disclose that the instruction groups (instruction streams) follow a simultaneous multi-threading structure (col. 2, lines 65-68).

14. In regard to claims 12 and 18, Hirata et al. further disclose that the instruction groups are prioritized to prevent pipeline failures (resulting from contention) during execution of instructions (col. 7, 65-68; col. 8, 1-10).

Response to Arguments

15. Applicant's arguments filed 01 September 2004 have been fully considered but they are not persuasive. Applicant argues in essence on pages 6-7 "...Hirata does not disclose delivering instructions using centralized dispersal logic within a scheduler via an operation bus...". This

has not been found persuasive. Hirata teaches in column 6, lines 11-14 and 25-34 and shows Figure 2(a), Figure 2(b), and Figure 3 that the scheduler receives the decoded instructions and distributes them to the functional units according to the instruction type. Figure 3 shows the instruction schedule unit, 15, is the sole scheduling unit to distribute the instructions from the individual fetching areas to the execution area. The instruction setup units are the fetch and decode areas, not the scheduler. The scheduler receives the instructions from each fetch and decode area and distributes the instructions according to type and priority. The operation bus is the connection between the schedule unit and the operation units, as shown in Figures 2(a), 2(b), and 3.

Conclusion

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J Li whose telephone number is (571) 272-4169. The examiner can normally be reached on M-T 7:30am-5:00pm.

17. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

18. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AJL
Aimee J. Li
16 December 2004

RICHARD L. ELLIS
PRIMARY EXAMINER